ENHANCED DYNAMIC PERFORMANCE IN SINGLE-PHASE CASCADED H-BRIDGE MULTILEVEL INVERTERS USING A NOVEL CONTROLLER

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ABSTRACT: Using closed loop controllers, this study examines the dynamic and steady state performance of a cascaded H-Bridge multilevel inverter (CHBMLI). A dual loop cascaded controller is suitable for an MLI system to address a range of issues. It consists of two loops: an inner loop and an outer loop. Proportional-Integral (PI) controllers are utilised as voltage controllers in the outer loop while proportional (P) controllers are used as current controllers in the inner loop. A current controller can reduce the time needed to reach steady state, or the transient/dynamic period, whereas a voltage controller can help achieve steady state voltage, or a constant output voltage. They use the same controller for both linear and nonlinear loads. The MATLAB/SIMULINK platform is used in this study to develop the closed loop CHB-MLI model, and the controller parameters integral gain (Ki) and proportional gain (Kp) are carefully selected. By varying these two parameters in both loops, the steady state and dynamic performance of a CHB-MLI for linear load may be determined. Stable state performance under non-linear load is investigated using the same controller and controller parameter settings as for linear load.

Keywords: Dual Loop Cascaded Controller, CHB-MLI, Non-linear Load, Linear Load, and Dynamic Performance

1. Introduction

The invention of the CHB-MLIhas been widely using diverse applications. MLIs was commonly used for high but medium-voltage applications [1]. That important usage of MLIs is electric drives,footing, the HVDC, the Renewable Root Frameworks utilities interface including STATCOM [2, 3]. Although the MLIs have many gadgets and parts and involve exposure circuits, their accompanying highlight becomes essential and useful, a) Low THD in voltage production due to the waveform output chance.b) Lower concern dv/dt on gadgets, contributing to decreased issues of EMI/EMC.c) Lower drawback trading owing to the lower frequencies exchange.d) Low voltages of simple mode.

Customary areas of MLI include NPC, Flying Conductor (FC) and MLIs flying via H-Bridge (CHB) [2-3]. The need for strength parts (power switches, input DC condensers, and supplementary DC condensers) often rises throughout the customary MLIs, as that of the volume of level increases. For example, eight switches, four DC-Condensors, and six intensity diodes are needed for a traditional 5-level diode MLI [4]. For example. In all cases, 16 force switches as well as eight DC input condensers are required for both the conventional 9-level diode clipped MLI[5] just one huge addition to the number of intensity segments over the NPC five-level. The increased amount of strength switches provides the pre-condition and protection for driver circuits. The increasing amount of DC capacitors needs additional voltage change circuits that minimise the efficacy of both the structure and increase the weight, bulky and varied design of both the frame. Throughout the exhibition sense, the usage of an MLI with whatever

numerical voltage levels may also be anticipated, as expected under the circumstances, is consistently appealing.

2. Literature survey

With this unusual scenario, analysts have been looking to increase the number of levels with both the least strength sections (for example, switches, condensers) with newly updated MLI geographiesaround 9 levels. That key aim of these topologies was to deliver greater excellence for the least imaginable power and a less complicated approach for regulating/control. The creator in [6] suggested an MLI landscape of nine stages of eight DC sources of knowledge and 16 force switches. It is quite concerning the proximity of the growing amount of strength pieces throughout this MLI. In[7] authorshave suggested a 9-level MLI to reduce the intensity section. It consists of 14 force switches including four DC sources of knowledge. Some may be bi-directional amongst these force switches. A comparison, a number of creators [8] suggested a nine-level MLI topology utilising fewer control switches to even further reduce the amounts of strength sections. Twelve intensity switches and four info source dc are needed for this nine-stage geography. Another specialist [9] found an integrated MLI geography with a single data DC source. Nevertheless, this geographic region uses several assistant condensers but one of these condensers' voltage instructions is an uncomfortable business.

Even, some scientists also proposed MLI geographies which compel assistant condensers to establish a stalled voltage of production [10-18]. These include MLI [10,11], MLI [12,13], dynamic nonpartisan point clipping dynamic capacitor (FC-ANPC) [12,13], including MLIs [14-17] for dynamic flight mixture dependent on condensers (FC- HANPC). That FC-ANPC MLI consists of multiple switches and assisting condensers, which involve complex controls to guide the voltage via the assisting condensers. Many supporting condensers, such as FC-ANPCMLI, are also being used in the NNPC MLI and FC-HANPCMLI, which expand mostly on multifaceted concept. Some designers have chipped away with the medium voltage and high power measured staggered converters (MMC) but additionally they need various supporting condensers [18-21]. MMCs often require complicated voltage measurements through helper condensers. Some experts have suggested MLI couplings [22-24], which need less force switches, but these designs require more voltage correction circuits to change the voltages through the DC knowledge condensers.

The whole paper suggests another 9-level (H9LI) Combination Geography to fix weaknesses, such as the high regulation of electricity switches, assistant condensers and Boost converters in current MLI geographies. H9LI's main aim is to achieve low section tally AC output voltage for low or zero distortion. The performance voltage of 9 levels is accomplished by means of less force switches contributing to easy power, low maintenance and above all improved reliability. That geography suggested involves the advantages of MLI diode-braced, MLI condenser-cutting and ML I coupling. The essential desirable conditions of the H9LI are outlined as follows:It uses less force switches (only 10 switches each leg of phase).Only one DC condenser and two DC condensers are necessary.It uses a wired inductor to decrease the need for DC condensers. The DC condensers have a short-predicted lifespan.The geography of the auxiliary condenser voltage is fitted with characteristic instructions. There is no requirement for more existing sensors.Bottom simple voltage function.This could support the frame responsively, enabling LVRT (low-voltage travelling).

The reduction in the number of switches and auxiliary condensers is done by either a coupled inductor consolidation. Even though the coupled inductor is typically not suitable for all sorts of applications, it is efficient. The condensers are known as the weak connection between the electrical device and the switches form the most vulnerable component of the system. Increasing switch requires a new controller device, which improves help as well as the total circuit cost, next to the insurance circuit. Reducing the number of gadgets regulated renders topology robust and competent.

3. Proposed Model

This section gives the detailed analysis of proposed model of CHB-MLI.Input side voltage level are usually obtained from RES so we are taking PV source as dc input. DC input given to the cascaded H bridge multi-level inverter with the help of switching frequencies the output voltage and output current are obtained. LC filter which reduces the voltages ripple as well as current

ripple. The outer loop controller is the PI controller is used as voltage controller to maintain the constant output voltage at any instant of load.The inner loop controller is the P controller is used as current controller to get the sinusoidal current at the load side. Pulse width modulation technique is used as a phase disposition level shifted PWM technique which implemented with carrier signal and reference signal.

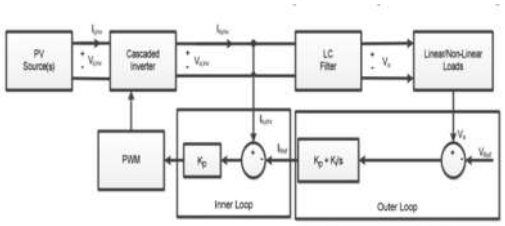

Figure 1. Proposed block diagram.

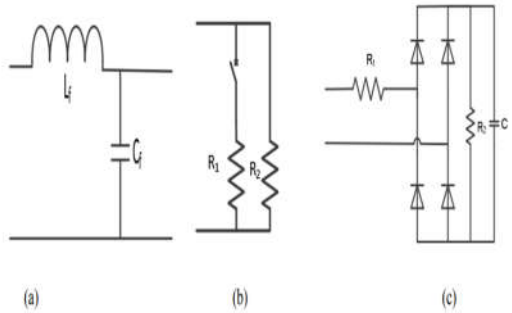

Figure2. (a) LC filter, (b) linear load and (c) non-linear load.

The suggested system is developed as seen in Figure 1. The PV panel supplies the DC input voltage to the CHB inverter. Additionally, an LC-filter is employed to lessen voltage and current ripple. The loads are supplied filter output (both linear and non-linear). As shown in Figure 2, the PI controller receives the input from the load and outputs it to the inverter for PWM switching. A sine wave and a triangle wave (carrier signal) are used in the PWM method (control signal or reference signal). The output of the inner loop controller serves as the PWM reference signal.

While the inner loop controller, the P controller, is used as a current controller to get sinusoidal current at the load side, the outer loop controller, the PI controller, is utilized as a voltage controller to maintain the constant output voltage at any moment of load. The LC filter, linear loads, and non-linear loads employed in the proposed system are shown in Figure 2(a). A switch is connected in series with R for an external load change, as illustrated in Figure 2(b). As shown in Figure 2, the load has changed throughout the simulation, causing the switch to turn on at 0.205 seconds in order to check the load voltage following the load change (b). A diode bride is employed as a non-linear load in Figure 2(c), and output voltage is measured across terminal AB. An outer loop voltage controller is used to keep the maximum output voltage constant even when the load changes, while an inner loop current controller is used to obtain sinusoidal current at the load side.

3.1 CHB-MLI

In this part, a five-level inverter with two cascaded bridges, also known as a CHB-MLI, is taken into consideration. This inverter's output voltage levels are 2Vdc, Vdc, 0, -Vdc, and -2Vdc [2]. Table 1 displays the switching states. In Figure 3, the output voltage (VAB) is provided by and the input voltages (v1 and v2) are two solar panels.

$$V_{AB} = V_{o1} + V_{02} \quad (1)$$

Pulse width modulation (PWM) is utilized to create the switching states shown in Table 2 of the switching process. The optimal modulation approach for MLI is the Phase Disposition Level Shifted (PD-LS) PWM technique. With a modulation index of 0.9 and a carrier signal of 1 kHz, this PWM method is applied to a reference signal of 50 Hz. Formula for modulation index (m_a) is given in (2).

$$m_a = \frac{V_{ref}}{V_{car}} \quad (2)$$

Here, V_{car} indicates the magnitude of the carrier, or the peak of the triangle wave, and V_{ref} represents the magnitude of the reference, or the peak of the sine wave.

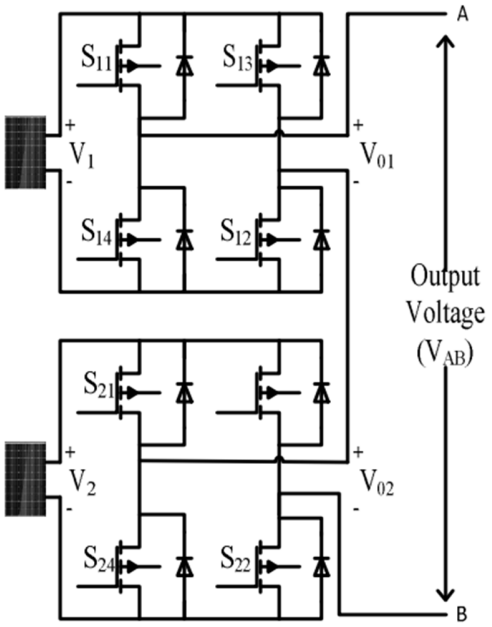

Figure3. Configuration of 5-level CHB-MLI.

TABLE I: SWITCHING STATES OF THE INVERTER

Switches / V_{AB}	Inverter 1 (V_1= V_d)				Inverter 2 (V_2= V_d)			
	S_{11}	S_{12}	S_{13}	S_{14}	S_{21}	S_{22}	S_{23}	S_{24}
2Vdc	ON	ON	OFF	OFF	ON	ON	OFF	OFF
Vdc	ON	ON	OFF	OFF	OFF	ON	OFF	ON
0	OFF	ON	OFF	ON	OFF	ON	OFF	ON
-Vdc	OFF	OFF	ON	ON	OFF	ON	OFF	ON
-2Vdc	OFF	OFF	ON	ON	OFF	OFF	ON	ON

3.2 CHB-MLI

There are many different methods for producing pulses for electronic semiconductor switches, including linear methods, non-linear methods (such as neural networks and fuzzy logic), and hysteresis band methods. Some of these methods include: (HB). For the purpose of controlling the voltage that is produced by the UPQC, the multilayer adaptive hysteresis band, abbreviated as ML-AHB, is provided here. This particular method of modulation is distinguished by its lightning-fast reaction, its pinpoint precision in tracking capabilities, and its low ripple. It is important to note that the bandwidth is a variable that may be determined theoretically or through the use of approaches that use artificial intelligence.

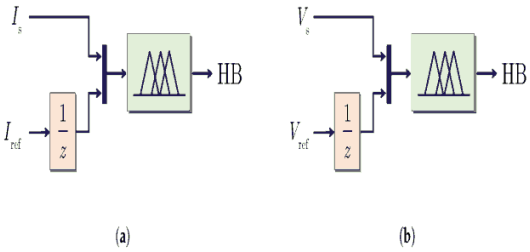

Figure 4. Calculating the Adaptive Hysteresis Band (HB) using fuzzy logic: (**a**) for current and (**b**) for voltage.

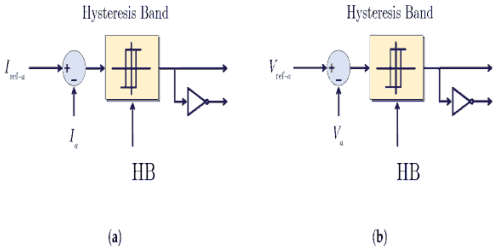

Figure 5. The generation of pulses for both parallel (**a**) and series (**b**) converters of phase a through AHB.

First, the fuzzy logic controller receives the signal for the source voltage (Vs), followed by the signals for the reference voltage and current (Vref, Iref). After that, the Adaptive Hysteresis Band is derived from the output of the fuzzy logic controller, as is seen in figure 4. The steps involved in producing the pulses for the parallel and series converters of phase (a) are shown in Figure 5a and Figure 5b, respectively.

One example of a non-linear and intelligent kind of controller is known as the fuzzy logic controller. The rules of the FLC are derived from the system parameters without the mathematical model of the system. The FLC takes a linguistic control strategy that is based on expert knowledge and turns it into an automated control strategy. This results in the system being more stable. The FLC is made up of three components: the fuzzification system, the inference system, and the defuzzification system. The fuzzy variables are represented using the membership functions as their descriptors. In situations where the output consisted of numerical values, the Sugeno technique of fuzzy logic was used. Figure 4a and Figure 4b, respectively, illustrate the membership functions of error and change in error that are associated with the proposed model. In the system that has been suggested, Gaussian membership functions have been chosen to

act as the inputs. The capacitor's voltage faults that occurred while the inverter was operating were sent to the FLC as its input. After that, the output of the FLC was multiplied in order to synchronize the supply voltage signal sin with the reference current of the APF using the phaselocked loop (PLL). Then, is was compared with is * to make the reference voltage signal (refer Figure 3). This reference voltage was compared with the carrier signals, which are combined with voltage balancing to form the PWM pulse for gating the switches of SSI. This pulse is used to control the flow of current through the switches. The current from the SSI is injected at PCC to compensate the current.

4. Results and discussions

This section gives the detailed analysis of simulation results implemented using Matlab/Simulink model. The controller parameters such as Kp and Ki are used to control CHB-MLI.The dc input voltage to the CHB inverter is taken from a solar panel. A five level Inverter is considered with two number of bridges were cascaded which is called as CHB-MLI with input voltage is of 100 volts.

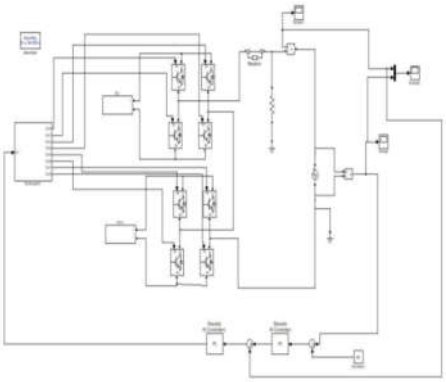

Figure 6. Simulink model of propose method.

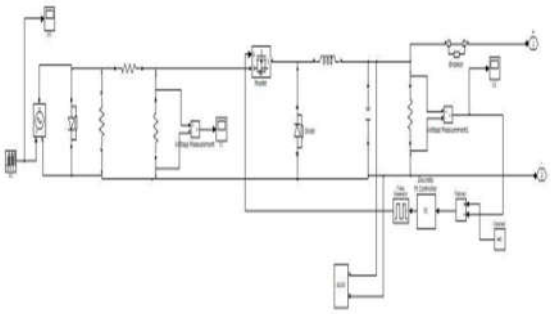

Figure7. Simulink model of PV panels.

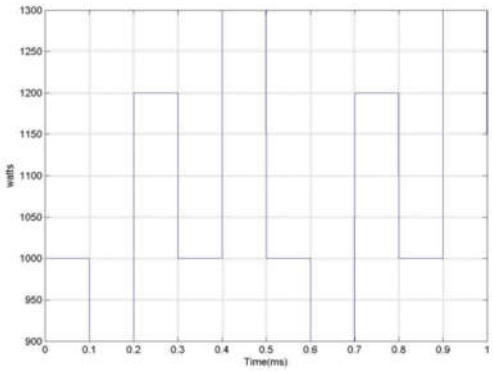

Figure 8. Simulation output of PV panel.

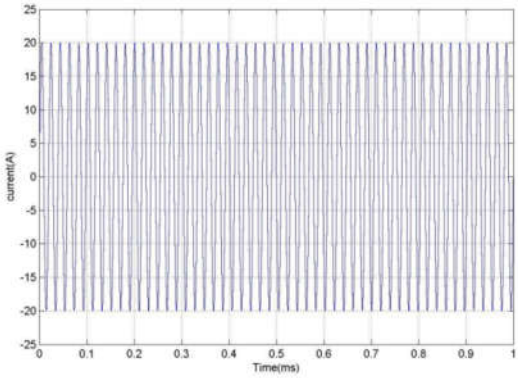

Figure 9. Simulation output of current.

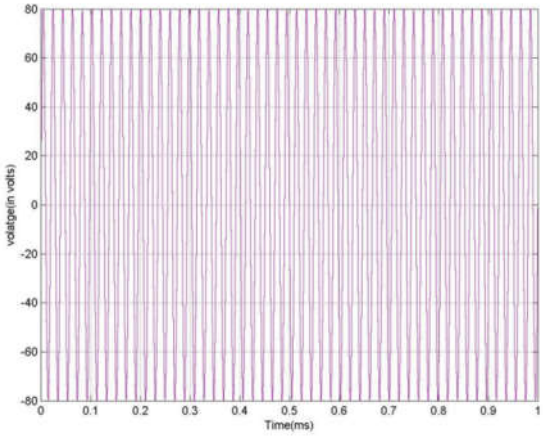

Figure10. Simulation output of voltage.

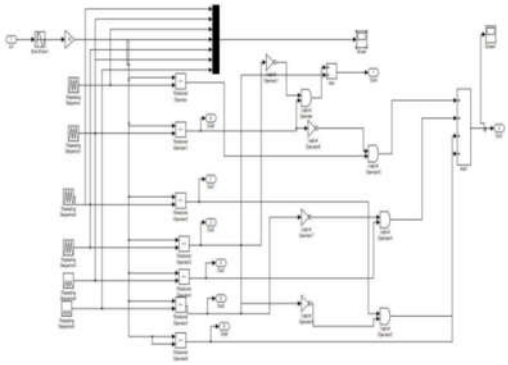

Figure 11. Simulink model of PWM technique

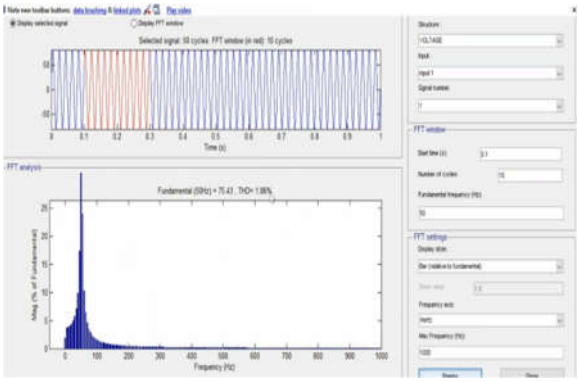

Figure 12. THD analysis for PI controller with output voltage.

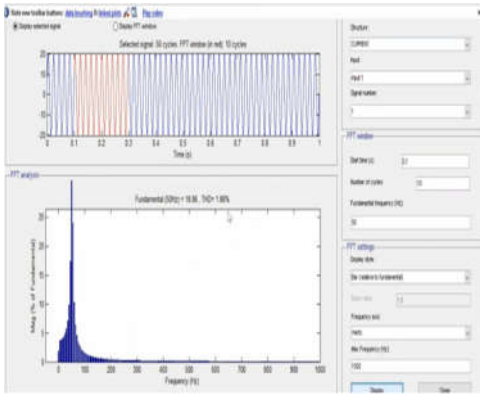

Figure 13. THD analysis for PI controller with output current.

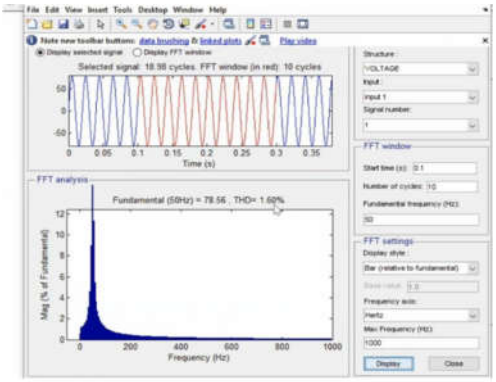

Figure 14.THD analysis for Fuzzy controller with output voltage.

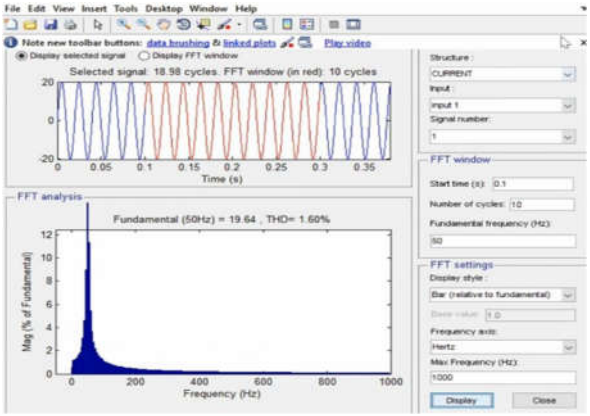

Figure 15. THD analysis for Fuzzy controller with output current.

Controller	THD of output voltage	THD of output current
PI controller	1.86%	1.86%
Fuzzy Controller	1.6%	1.6%

Table 2. THD performance comparison

5. Conclusion

A symmetrical CHB-MLI using PD-PWM technique has been analyzed in this work.Both Inverters consist of same power semiconductor switches but output voltage levels are different. In this system the THD is very less in symmetrical CHB-MLI with fuzzy logic controller and it is implemented in real time system using MATLAB with R load.This type of proposed system is used for high power applications in photovoltaic and it reduce overall cost as well as size of the system. This work can be extended with hybrid CHB-MLIs with deep learning controllers for improved performance.

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