ENHANCING NOISE RESILIENCE IN CMOS DYNAMIC LOGIC: ON-CIRCUIT METHODOLOGIES

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ABSTRACT

In order to achieve very high system performance, dynamic CMOS logic circuits are commonly used in high-performance VLSI chips. Dynamic CMOS gates, on the other hand, are fundamentally less noiseresistant than static CMOS gates. Due to the increasingly demanding noise requirements imposed by aggressive technological scaling, the noise tolerance of dynamic circuits must first be enhanced in order for VLSI chips created utilising deep submicron process technology to operate reliably. A number of design strategies for improving the noise tolerance of dynamic logic gates have been proposed in the literature. This study begins with an overview and classification of these strategies. Then, employing circuitry that exhibits a negative differential resistance effect, we present a unique noise-tolerant design technique. Through study and simulation, we have shown that employing The noise tolerance of dynamic logic gates can be enhanced beyond that of static CMOS logic gates using the proposed technology, while the performance advantage of dynamic circuits is preserved. The input noise immunity level can be improved to 0.8 V for about 10% delay overhead and to 1.0 V for only about 20% delay overhead at a supply voltage of 1.6 V, according to simulation results on large fan-in dynamic CMOS logic gates.

INTRODUCTION

DIGITAL integrated circuit noise has become one of the foremost issues in the design of very deep submicron VLSI chips [1], [2]. Noise in digital integrated circuits refers to any phenomenon that causes the voltage at a node to deviate from its nominal value. While these noises always existed, in the past they had little impact on the performance of integrated circuits and were often neglected. It is the unstopped aggressive technology scaling in an effort to continuously improve chip performance and integration level that makes noise play an increasingly important role in comparison with conventional design metrics like area, speed, and power consumption.

Together with technology scaling, aggressive design practices like employing dynamic logic styles have also seen wider use in recent years to achieve higher performance of integrated cir- cuits. Circuits designed using dynamic logic styles can be con- siderably faster and more compact than their static CMOS counterparts. This is especially the case with wide fan-in dynamic logic gates where a single gate can realize the logic function that otherwise would require multiple levels of static CMOS logic gates. Therefore, wide fan-in dynamic gates are routinely employed in performancecritical blocks of high-performance chips, such as

in microprocessor, digital signal processor, and so on.

Criticism on dynamic circuits is often related to their rela- tively poor noise tolerance. The switching threshold voltage of a dynamic CMOS logic gate, defined as the input voltage level at which the gate output changes state, is usually the transistor threshold voltage . In comparison, the switching threshold voltage of static CMOS logic gate is typically around half the supply voltage. Therefore, dynamic logic gates inherently have less noise immunity than static CMOS logic gates and are the weak link in a high-performance VLSI chip designed using deep submicron process technology.

A number of design techniques have been developed in the past two decades in an effort to reinforce this weak link. For ex- ample, feedback keepers were proposed to prevent the dynamic node from floating; internal nodes were precharged to eliminate the charge sharing problem; and weak complementary pnet- work is constructed to improve the noise tolerance to the level of skewed static CMOS logic gates. However, existing remedial techniques improve dynamic circuit noise tolerance at a signif- icant cost in terms of one or more other important design met- rics like circuit area, speed, and power consumption. The fact is that the amount of overhead increases dramatically when the noise tolerance requirement is increased along with the contin- uous down-scaling of the process technology. Therefore, effec- tive noisetolerant design techniques that incur little overhead in silicon area, circuit speed and power consumption are highly demanded.

In this paper, we propose a novel design method to enhance the noise tolerance of dynamic circuits. We will show that dy- namic logic gates are not necessarily less noise tolerant if proper noise-tolerant design techniques are employed. In fact, using the proposed method in this paper, noise tolerance of dynamic logic circuits can be improved beyond the level of static CMOS logic gates while still retain their advantage in performance.Further- more, in contrast to most previous papers which describe only one new circuit in a paper, the proposed noise-tolerant design method can be realized using a number of different circuits and therefore having broader impact.

The rest of this paper is organized as follows. Section II briefly explains various noises sources in dynamic logic circuits designed using deep submicron process technology. Section III presents an extensive overview and classification of existing noise-tolerant design techniques. In Section IV, the proposed noisetolerant design method is described. The noise margin

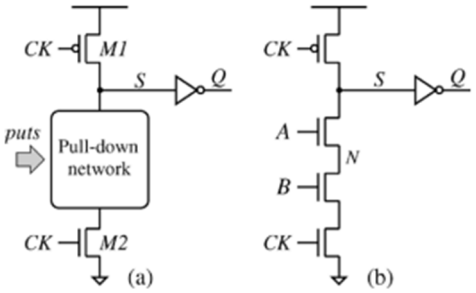


Fig1. Domino logic gate. (a) Circuit schematic. (b) Two-input AND gate

And delay of dynamic circuits using the proposed technique are analyzed in Section V. In Section VI, experimental results on wide fan-in domino gates based on HSPICE simulation are presented.

NOISES IN DYNAMIC LOGIC CIRCUITS

For ease of presentation, in this paper our discussion will be focused on one type of dynamic circuits known as domino CMOS

logic circuits [3], which is probably the most widely used dynamic logic style. However, it is noted that the noise- tolerant design techniques discussed in this paper can also be applied to other types of dynamic circuits.

A typical n-type domino CMOS logic gate, as shown in Fig. 1(a), consists of clock controlled transistors M1 and M2, a pull-down n-type transistor network, and an output driver. The operation of a domino CMOS logic gate can be divided into two phases. In the precharge phase when the clock CK is low, the dynamic node S is charged to logic high through M1 and the output of the gate Q is low. The evaluation phase starts when the clock goes high. In this phase, M1 is OFF and M2 is ON. The dynamic node S discharges or retains

its charge depending on the inputs to the pulldown network. An example 2-input domino AND gate is illustrated in Fig. 1(b). Noise sources in dynamic logic circuits can be broadly classi- fied into two basic types: i) gate internal noises, including charge sharing noise, leakage noise, and so on and ii) external noises, including input noise, power and ground noise, and substrate noise.

1) Charge sharing noise is caused by charge redistribution between the dynamic node and the internal nodes of the pull-down network. Charge sharing reduces the voltage level at the dynamic node causing potential false switching of a dynamic logic gate.

2) Leakage noise refers to the possible charge loss in the evaluation phase due to subthreshold leakage current. Leakage current increases exponentially with respect to transistor threshold voltage, which is continuously being down-scaled as the power-supply voltage reduces. Therefore, leakage in transistors can be a significant source

of noise in wide dynamic logic gates designed using very deep submicron process technology.

3) Input noise refers to noise presented at the inputs of a logic gate. They are primarily caused by the coupling effect, also known as crosstalk, among adjacent signal wires. This type of noise has become a prominent source of failures for deep submicron VLSI circuits because of the aggressive interconnect scaling in the lateral dimen- sions with relatively unchanged vertical dimensions.

4) Power and ground noise is mainly caused due to the par- asitic resistance and inductance at the power and ground networks and at the chip package. Power and ground net- works can also be contaminated by external noises from chip pins. Besides obviously reducing gate noise margin due to possibly lowered supply voltage, the power and ground voltage mismatch between a driver gate and a re- ceiver gate can translate to a dc noise at the input of the receiver.

5) Substrate noise can affect the signal integrity of a logic gate through substrate coupling. Furthermore, since tran- sistor threshold voltage is a function of the substrate voltage, noise in the substrate can momentarily lower the threshold voltage of the transistors in the pull-down net-work rendering them more susceptible to other noises.

In all, those noises, together with other sources of disturbance like process variation, alpha particle radiation, and so on, can en- danger the correct function of dynamic logic circuits designed using very deep submicron process technology. And a desired noise-tolerant design technique should be able to improve the noise

immunity of dynamic logic gates against all afore-men- tioned noises.

OVERVIEW OF PREVIOUS WORKS

In the past two decades, a number of circuit techniques have been developed with a view to improve the noise immunity of dynamic CMOS logic gates. While it is impractical to include every technique in the literature, in this section we present an overview of some significant techniques. And we have classified those techniques into four main categories based on the principle of their operations: 1) using keeper; 2) precharging internal nodes; 3) raising source voltage; and 4) constructing complementary p-network.

Employing Keeper

Perhaps the simplest way to enhance the noise tolerance of dynamic CMOS logic gates is to employ a weak transistor, known as keeper, at the dynamic node as shown in Fig. 2. The keeper transistor supplies a small amount of current from the power-supply network to the dynamic node of a gate so that the charge stored in the dynamic node is maintained. In the original domino dynamic logic work [3], the gate of the pMOS keeper is tied to the ground, as shown in Fig. 2(a). Therefore, the keeper is always on. Later, feedback keepers, illustrated in Fig. 2(b), became more widely used because they eliminate the potential dc power consumption problem using the alwayson keeper in the evaluation phase of domino gates [4].

The use of keeper causes contention when the pull-down network is ON during the evaluation phase, resulting in slower overall gate performance. In wide fan-in gates designed using very deep submicron process technology, the large leakage current through the n-network necessitates a very strong keeper to retain the voltage at the dynamic node. To reduce the serious contention problem associated with the strong keeper, new keeper design techniques have been recently proposed by Anis

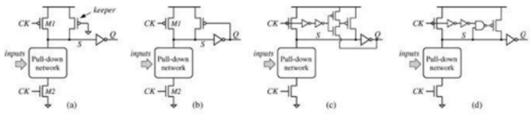


Fig2. Improving noise immunity of dynamic logic gates using keeper. (a) Weak always-on keeper [3]. (b) Feedback keeper [4]. (c) HS feedback keeper [5]. (d) Conditional feedback keeper [7].

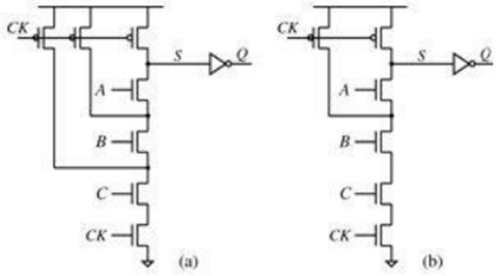


Fig3. Precharging internal nodes (3-input AND gate). (a) Precharge all internal nodes [9]. (b) Partial precharge [10].

In chip area and in clock load. NMOS transistors can also be used to precharge the internal nodes if the cost of an inverter to generate the complementary clock signal can be justified. Since the internal nodes are only precharged to, dynamic logic gates using nMOS precharge transistors have reduced discharging time and decreased dynamic power consumption. Fi- nally, it is noted that techniques based on precharging internal nodes alone are not very effective against external noises. et al. in [5] and [6] [see Fig. 2(c)] and Alvandpour et al. in [7] and [8] [see Fig. 2(d)]. Both techniques share the same basic principle, that is, to temporarily disable the keeper during the small time window when the dynamic gate switches. These two techniques have been shown to be very effective in enhancing

the noise tolerance of dynamic gates against gate internal noises

like leakage noise. However, dynamic gates with those keepers are still susceptible to external noise glitches because the dynamic node is not adequately protected during the gate switching time window. We will explain this in detail in Sec- tion IV and show a novel class of keeper design techniques that increases gate noise immunity against both internal and external noises with minimal contention.

Precharging Internal Nodes

In complex dynamic logic gates with large pull-down net- work, charge sharing between the dynamic node and the in- ternal nodes in the pull-down network often results in false gate switching. A simple yet effective way to prevent the charge sharing problem is to precharge the internal nodes in the pull- down network along with precharging the dynamic node S [9], [10]. An example dynamic 3-input AND gate using this tech- nique is illustrated in Fig. 3(a). When all internal nodes are precharged, this technique is able to eliminate the charge sharing problem at the cost of using a large number of precharge transis- tors and the increased load capacitance on the clock net. Partial precharge, as shown in Fig. 3(b), has also been used in design practice as a tradeoff between noise immunity and overheads.

Raising Source Voltage

One effective way to improve noise tolerance against both in- ternal and external noises is to increase the source voltage of the transistors in the pull-down network. Since the gate voltage has to be greater than the sum of the source voltage and the tran- sistor threshold voltage when a transistor is turned on, higher source voltage directly leads to increased gate turn-on voltage. Furthermore, due to the body effect, transistor threshold voltage is increased when the source voltage rises. This also contributes to improving gate turn-on voltage.

The pMOS pull-up technique [11], shown in Fig. 4(a), employs a pMOS transistor at node N2 forming a resistive voltage divider with the bottom clock controlled transistor. The voltage at node N2, which determines the switching threshold voltage of the dynamic logic gate, can be adjusted by changing the relative size of the pMOS pull-up transistor. One major drawback of this technique is the dc power consumption in the resistive voltage divider. Furthermore, since the voltage level at the dynamic node S can never get lower than the voltage at node N2, the voltage swing at node S is not rail-to-rail. When the size of the pMOS pull-up transistor is large in an effort to aggressively raise gate noise immunity, the gate output may also not have a rail-to-rail swing.

An improved method, shown in Fig. 4(b), employs a pull-up transistor with feedback control [12]. Here an nMOS transistor M1 is used to pull up the voltage of an internal node. The gate of the pull-up transistor is connected to the dynamic node of the domino gate. This design allows the pull-up transistor to be shut off when the voltage of the dynamic node goes low, therefore, the dynamic node S undergoes rail-to-rail voltage swing. Also, the dc power consumption problem is partially solved. It occurs only under certain input combinations that do not turn on the pull-down network. Note that a pMOS transistor can similarly

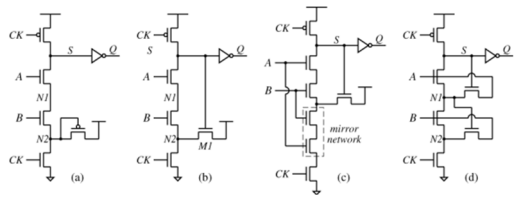


Fig4. Raising source voltage (2-input AND gate). (a) pMOS pull-up technique [11]. (b) NMOS pull-up (with feedback) [12]. (c) Mirror technique [13]. (d) Twin transistor technique [15].

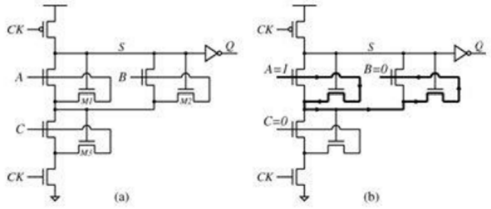


Fig5. Possible short circuit problem using twin transistor technique. (a) A 3-input OR-AND gate. (b) Direct conducting path.

Be used in this technique provided that the gate of the pMOS transistor is connected to the output of the dynamic logic gate. The mirror technique , employs a feedback controlled nMOS transistor similar to the nMOS pull-up technique. In addition, it duplicates the pull-down network in an effort to further reduce dc power consumption and to further improve gate noise tolerance. A 2-input dynamic AND gate designed using the mirror technique is shown in Fig. 4(c). Whenever the pull-down network is OFF, the mirror network is also OFF, hence, cuting off the potential dc conducting path from the nMOS pull-up transistor through the bottom clock controlled transistor. Therefore, the dc power consumption problem is completely solved. However, this technique significantly lengthens the discharge path in the pull-down network, which potentially leads to slower circuit or considerably increased circuit active area when the transistors are aggressively sized.

The twin transistor technique [15], [16] adopts nMOS pull-up transistors at all internal nodes to further improve dynamic gate noise immunity. In addition, the drain nodes of the pull-up nMOS transistors are connected to the inputs instead of to the power-supply network, as illustrated in Fig. 4(d). By doing so, unnecessary injection of current by the pull-up transistors is avoided, resulting in lower gate power consumption. However, this technique leads to increased gate input capacitance which may slow down the switching of the gates in the previous stage. Further, this technique is not suitable for certain logic functions because it may short input nodes. As an example, in Fig. 5(a) we show a 3-input OR-AND gate implementing the logic function of . Assume input A is high while inputs B and C are low. The dynamic node S stays high because C is low and there is no discharging path to the ground. Under such scenario, there is a dc conducting path between the two inputs A and B, as illustrated in Fig. 5(b). Therefore, the logic states at node A or node B are unclear. Note that the resulting damage can go far beyond the single dynamic gate understudy if these ambiguous nodes feed to a large number of other gates.

Constructing Complementary p-Network

The basic principle of this class of techniques is to construct a weak complementary pnetwork to prevent the dynamic node from floating in the evaluation phase. One such technique ,is illustrated in Fig. 6(a). The gate operates in a similar way as a normal domino gate in the precharge phase. In the evalua- tion phase, the logic gate behaves as a skewed CMOS logic gate. Therefore, the switching threshold voltage of the dynamic logic gate is equivalent to that of a skewed CMOS

logic gate. In ad- ditional to the silicon area overhead associated with the pull-up network, a major drawback of this technique in practice is its in- effectiveness in dealing with very wide logic gates, for example, wide OR gates, where dynamic logic styles really outshine static CMOS logic gates in performance.

PMOS transistors can also be employed at a per transistor level, as shown in Fig. 6(b). This technique is known as CMOS inverter technique [19]. The relative size of the pMOS transis- tors can be varied to adjust the switching threshold of the dy- namic logic gate. One advantage of this technique is that it can be selectively applied to a subset of inputs if they can be identi- fied as noisy in advance. The main drawback of this technique is that it is not suitable for OR type logic gates because of possible serious dc currents under certain input combinations.

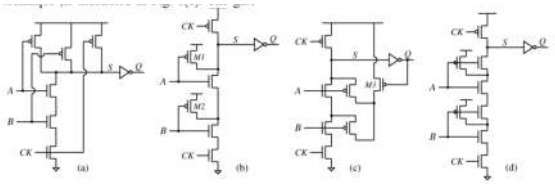


Fig6. Constructing complementary PFET network (2-input AND gate). (a) Complementary p-network technique . (b) CMOS inverter technique .(c) Gated CMOS inverter technique [20]. (d) Triple transistor technique .

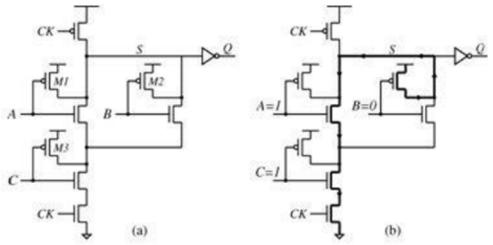


Fig7. Possible short circuit problem using CMOS inverter technique. (a) A 3-input OR-AND gate. (b) Direct conducting path.

When inputs A and C are high and input B is low, there is a direct con- ducting path between the power-supply network and the ground node, as shown in Fig. 7(b). More hazardous than the obvious problem of dc power consumption, the voltage at node S is de- termined by the relative strength of the pull-up transistor M2 and that of the transistors in the discharge path. The gate may fail to switch when the pull-up transistor is sized relatively strong in an effort to aggressively improve gate noise tolerance. Note that the dynamic node can be false reset with certain input combinations using either of the two above techniques. In Fig. 6(b), for example, if input A stays high and input B falls from high to low during the evaluation phase, the dynamic node may be reset to high by the pull-up pMOS transistor M2. With a view to solve this false reset problem, Evans in used an additional transistor M3, shown in Fig. 6(c). M3 is ON when the gate output remains low. When the evaluation is executed and the output rises, M3 is turned off disconnecting the pullup transistors from the power-supply network. Similar tactic can also be applied to improve the simple complementary p- network technique. It is noted that this gated CMOS inverter technique does not completely solve the dc conducting problem for certain logic circuits.

Fig. 6(d) illustrates a noise-tolerant 2-input AND gate using a triple transistor technique , where each nMOS transistor in the pull-down network of a simple dynamic logic gate is replaced by three transistors. The technique can be considered as a variation of the CMOS inverter technique where an additional nMOS transistor is used to prevent the possible dc conducting path problem in the evaluation phase. Similar to the mirror tech- nique, this technique significantly lengthens discharge paths in the pull-down

network. While it can be useful for certain logic gates like wide-OR gates, it is not practical to be applied to general pull-down nMOS network because of its overhead in circuit area and performance.

Comparison of Techniques

In this section, we compare the noise-tolerant design tech- niques described in the previous sections. We start by listing the set of basic requirements that a desirable noise-tolerant design technique should meet.

1) It improves gate noise tolerance against all types of noises.

2) It is suitable for all logic functions.

3) It has minimal circuit area overhead.

4) It has minimal circuit speed overhead.

5) It consumes no dc power and has minimal ac power con- sumption overhead.

Table I. Comparison Of Existing Dynamic Circuit Noise Tolerance Enhancing Techniques

Class	Technique	Reference	Illustration	Num. tran.	Input load[a]	Clock load[a]	Dischrg path[a]	DC current[a]	All noises[a]	All func.[a]
A	Always-on keeper	[3]	Fig. 2(a)	N	o	o	o	×	o	o
	Feedback keeper	[4]	Fig. 2(b)	N	o	o	o	o	o	o
	HS feedback keeper	[5]	Fig. 2(c)	N	o	o	o	o	×	o
	Conditional feedback keeper	[7]	Fig. 2(d)	N	o	o	o	o	^	o
B	Precharge internal nodes	[9]	Fig. 3(a)	2N	o	×	o	o	×	o
	Partial precharge	[10]	Fig. 3(b)	N	o	×	o	o	×	o
C	PMOS pull-up	[11]	Fig. 4(a)	N	o	o	o	×	o	o
	NMOS pull-up (feedback)	[12]	Fig. 4(b)	N	o	o	o	×	o	o
	Mirror technique	[13]	Fig. 4(d)	2N	×	o	×	o	o	o
	Twin transistor	[15]	Fig. 4(c)	2N	^	o	o	o	o	^
D	Complementary p-network	[17]	Fig. 6(a)	2N	×	o	o	o	o	o
	CMOS inverter	[19]	Fig. 6(b)	2N	×	o	o	o	o	×
	Gated CMOS inverter	[20]	Fig. 6(c)	2N	×	o	o	o	o	×
	Triple transistor	[21]	Fig. 6(d)	3N	×	o	×	o	o	o

[a]Symbol o represents 'good' and symbol ^ represents 'not good'.

Paths in the pull-down network is intact. The ninth column in- dicates whether the dynamic gate maintains the zero dc power consumption property. The tenth column shows whether the technique enhances noise tolerance against both internal and ex- ternal noises. And finally, the last column shows whether the technique can be applied to all logic gates.

It is shown in the table that the twin transistor technique and CMOS inverter based techniques are not suitable for all logic functions. Techniques based on precharging internal nodes as well as the two new feedback keeper techniques only improve gate noise immunity against certain types of noises. Both the pMOS pull-up technique and the nMOS pull-up (with feedback) technique consumes dc power. The Mirror technique and the triple transistor technique increase the length of gate discharge path. Techniques based on raising source voltage usually ei- ther have dc power consumption or require significantly larger silicon area. Techniques based on constructing complementary p-network often require larger silicon area and they increase the previous stage gate delay due to greater gate input capacitance. In all, simple feedback keeper is the only general-purpose technique that improve dynamic logic gate noise immunity against all types of noise without significant increase in silicon area (device count), speed, and power consumption.

PROPOSED NOISE-TOLERANT DESIGN TECHNIQUE

The simple feedback keeper technique is effective against noises and is easy to design. However, there is a fundamental dilemma in choosing the size of the keeper. On one hand, a strong keeper is required to achieve high gate noise tol- erance. On the other hand, large keeper leads to significant contention during normal gate switching, therefore deteriorates gate performance. The conditional keeper techniques [5]–[8] temporarily disable the keeper or reduce keeper strength to alleviate the contention problem. But dynamic gates equipped with those keepers are susceptible to input noise glitches be- cause the dynamic node is not adequately protected during the gate switching time window.

Noise immunity against input noises is very difficult to achieve without significant sacrifice in circuit performance because the gate should not act before it identifies whether the input is noise or real signal. This inevitable time needed to distinguish noise from real signal, which is obtained by monitoring the initial period of the input voltage waveform, causes degradation in circuit performance.

Basic Principle

First, let us carefully reexamine the noise tolerance versus speed conundrum. It may be observed that there is an ambi- guity in the definition of the strength of the keeper. The keeper strength that determines gate noise tolerance is not necessarily the same as the keeper strength that governs the gate performance. Let us measure the keeper strength in terms of the cur- rent supplied by the keeper.

Keeper strength that determines gate speed is approx- imately the average current when the applied voltage across the keeper is in the range [0,); this current is given by

$$I_{sp} = \frac{2}{V_{DD}} \int_0^{V_{DD}/2} I(V)dV. \quad (1)$$

• Keeper strength that determines gate noise robustness is the small-signal maximum current, defined as

$$I_{nm} = \max_{0 \le V \le V_D} (I(V)) \quad (2)$$

where is the maximum allowed voltage deviation from the ideal voltage at the dynamic node S and it is much smaller than in practice.

It is the difference between keeper strength for gate performance and keeper strength for gate noise immunity that makes it pos- sible to enhance the noise tolerance of a dynamic logic gate while still retaining its performance. We will hereafter call a keeper that aggressively exploresthis difference a smart keeper.

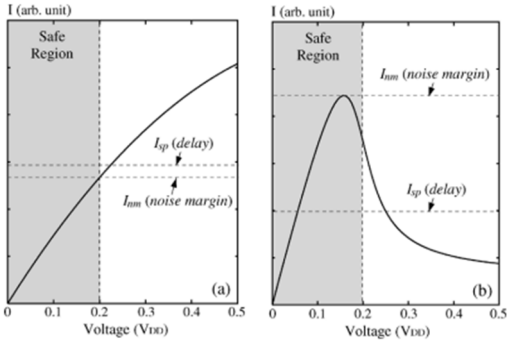


Fig8. Comparing keeper strengths for noise margin and for gate speed purposes. V = 0:2V . (a) Fieldeffect transistor.(b)Circuit or devicewith negative differential resistance region.

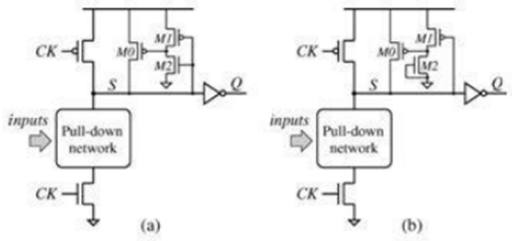


Fig9. Domino logic gate with optimized feedback keeper. (a) CMOS inverter feedback. (b) Pseudo-pMOS inverter feedback.

Theorem 2: If the – characteristic of a keeper is mo- notonously increasing and it is also concave, the ratio of delay keeper strength and noise keeper strength has a lower bound of The goal of circuit designers is, therefore, to find a keeper that has a large and, at the same time, a small . However, this goal is not able to be materialized using a single fieldeffect transistor, which has a monotonous – characteristic where the current always rises when the applied voltage across the transistor is increased. Using such device as the keeper, it can be shown that has a very loose lower bound of Theorem 1: If the – characteristic of a keeper is

monotonously increasing, the ratio of delay keeper strength and noise keeper strength has a lower bound of

Proof:

$$\geq \frac{2}{V_{DD}} \int_{V_D}^{V_{DD}/2} \frac{I(V)dV}{I(V_D)}$$

$$1 - V_D/V_{DD} \quad \frac{\frac{2}{V_{DD}} \left(I(V_D) \cdot \left(\frac{V_{DD}}{2} \quad V_D \right) \right)}{I(V_D)}$$

$$2\frac{V_D}{V_{DD}}.$$

l,mIn practice, this lower bound is a very loose one. To im- prove it, we further use the fact that the – characteristics of MOSFET devices are always concave. A function f(x) is:

Proof:

$$\frac{I_{sp}}{I_{nm}} = \frac{2}{V_{DD}} \int_0^{V_{DD}/2} \frac{I(V)dV}{\max\limits_{0 \leq V \leq V_D} (I(V))}$$

$$= \frac{\frac{2}{V_{DD}} \left(\int_0^{V_D} I(V)dV + \int_{V_D}^{V_{DD}/2} I(V)dV \right)}{I(V_D)}$$

$$\geq \frac{\frac{2}{V_{DD}} \left(\frac{I(V_D)}{2} V_D + I(V_D) \cdot \left(\frac{V_{DD}}{2} - V_D \right) \right)}{I(V_D)}$$

$$= 1 - \frac{V_D}{V_{DD}}.$$

For realistic MOSFET-based keeper, as shown in Fig. 8(a), the delay keeper strength is often comparable to, if not greater than, the noise keeper strength . I_{nm}.

Optimizing Conventional Keepers

We will first optimize conventional feedback keepers such that the keeper strength for speed is minimized when the keeper

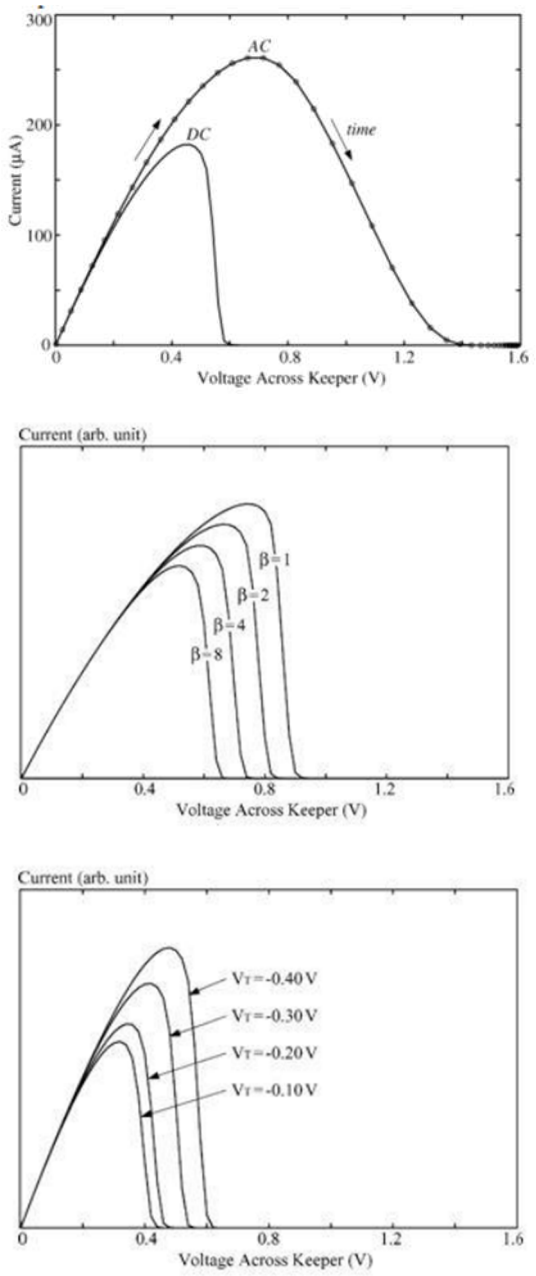


Fig10. Impacts of transistor sizing and threshold voltage on I–V characteristic. (a) With respect to beta ratio. (V = 0:40 V .) (b) With respect to threshold voltage (= 4:0).

Strength for noise tolerance (that is, the gate noise-tolerant re- quirement) is given. Fig. 9(a) shows a dynamic logic gate with the conventional feedback keeper. Here a weak CMOS inverter is employed to generate the feedback signal instead of directly connecting gate output Q to the gate node of transistor M0. This has at

least two advantages. First, the response time of the feedback process is independent of external gate load condition. Second, this gives us the freedom to independently optimize the feedback inverter without having to worry about the gate output. A variation of this design, where a pseudopMOS inverter feed- back is used, is shown in Fig. 9(b). Since both keepers operates similarly, we will focus our discussion on the first keeper de- sign. Characteristic of the keeper circuit is very sensitive to the parameters of the transistors. Since we want the keeper current to quickly drop when the voltage level at the dynamic node S decreases, the two most important parameters are: 1) the size ratio of the pull-up transistor M1 and the pull-down transistor M2 and 2) the threshold voltage of the pull-up transistor M1. In Fig. 10, we have plotted the impacts of beta ratio of the feedback inverter and the threshold voltage of M1 on the –characteristic of the keeper. Obviously, a large beta ratio and a low threshold voltage are preferred in this application.

Smart Keepers Designed Using MOSFETs

Circuits designed using MOSFET devices that exhibit the NDR property have been studied extensively in the literature [23], [24]. In fact, systematic methods have been developed to construct NDR circuits using transistors [24]. Those existing NDR circuits constitute a pool of potential circuits for MOSFET- based smart keepers. Here we will demonstrate how those NDR circuits can be employed in the keeper network by using one of the simplest of those NDR circuits.

This two-transistor simple NDR circuit, illustrated in Fig. 12(a), was first proposed in [22]. It is composed of a cross-coupled depletion-mode nMOS transistor M1 and depletion-mode pMOS transistor M2. Since the gate of M1 is connected to the dynamic node S, the current through the

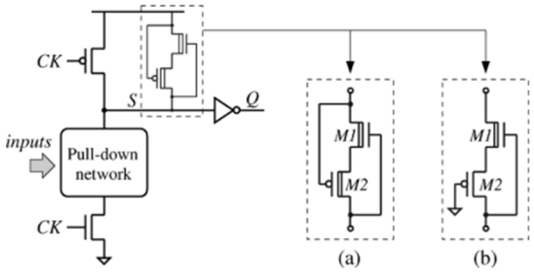


Fig12. Domino logic gates with MOSFET-based smart keeper. (a)Depletion-mode nMOS with depletion-mode pMOS. (b) Depletion-mode nMOS with enhancement-mode pMOS.

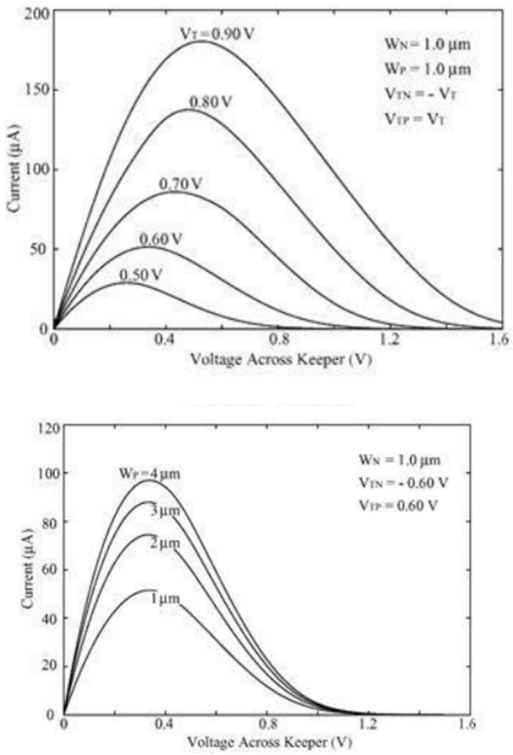
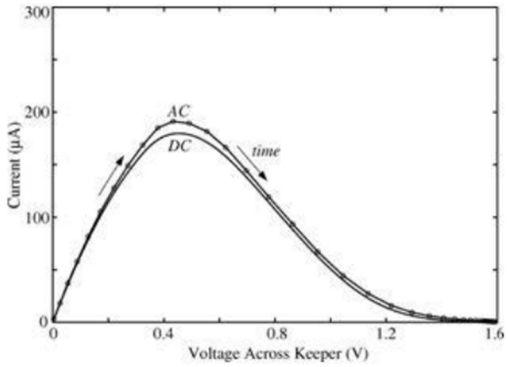


Fig13. Impacts of threshold voltage and transistor sizing on I–V characteristic. (a) With respect to threshold voltage. (b) With respect to transistor sizing.

Two transistors will be cut off immediately when the voltage at S drops to the turn-off voltage of M1. It is noted that in our application the gate of transistor M2 connects to a constant voltage source, the

power-supply node. Therefore, we can alternatively use an enhancement-mode pMOS transistor whose gate is connected to the ground node, as shown in Fig. 12(b).

The impacts of transistor threshold voltage and transistor sizing on the - characteristic of the circuit are shown in Fig. 13. It is observed that the current peak moves leftward



When the absolute value of the threshold voltage is reduced. However, at the same time the peak current value quickly de- creases meaning that significantly larger keeper size is required to retain the same gate noise tolerance level. When the relative size of the transistors is changed, it is also observed that even though the magnitude of the current changes, the shape of the – characteristic remains largely unchanged. A typical ac – characteristic of the proposed keeper, together with its corresponding dc – characteristic, is shown in Fig. 14. It can be seen that the two curves are very close to each other and they reach their peaks at approximately the same voltage value across the keeper. This is in distinct contrast to the case of the conventional feedback keeper discussed in the previous section (see Fig. 11). It is mainly because of the fact that the gate of transistor M1 is directly wired to the dynamic node S, therefore is able to cut off the current through the keeper instantaneously when the voltage at S drops. The slight difference between the two – curves is caused by the small amount of time required to discharge the parasitic capacitance of the internal node residing between the two transistors M1 and M2.

Smart Keepers Designed Using NDR Devices Smart keepers can also be realized using devices that intrin- sically have the foldedback - characteristic. The keeper can be either a three-terminal NDR device or series con- nected two-terminal NDR device and a feedback controlled MOS transistor, as illustrated in Fig. 15. Typical two-terminal NDR devices include tunneling diodes, resonant tunneling diodes, resonant-interband tunneling diodes, etc. And example threeterminal NDR devices are resonant-tunneling transistors, negative-resistance field-effect transistors, resonant-tunneling hot-electron transistors, etc. An extensive overview of semi- conductor devices including those having the NDR property can be found in [25].

In the paper, we will take the RTD+FET implementation as an example. RTDs are semiconductor heterostructures with a lowbandgap quantum well being sandwiched between two barrier layers of high-bandgap materials.

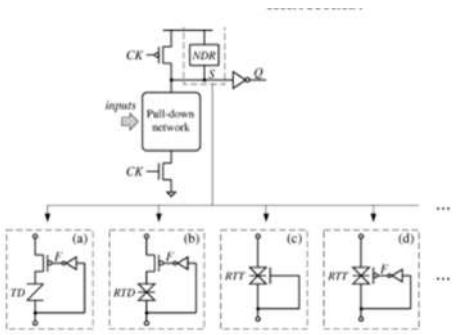


Fig15. Domino logic gates with smart keepers designed using intrinsic NDR devices. (a) Tunneling diode with MOS transistor. (b) Resonant-tunneling diode with MOS transistor. (c) and (d) smart

keepers based on threeterminal NDR devices.

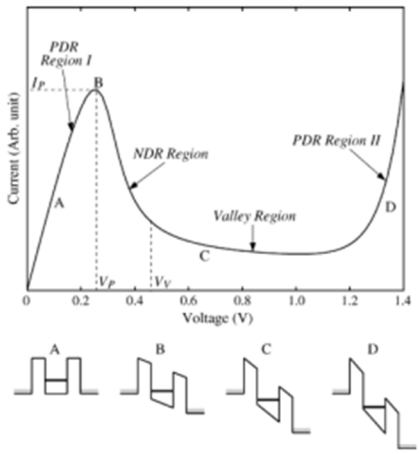


Fig16. Typical I-V characteristic of resonant tunneling diodes and schematic band diagrams

The narrow well are discretized due to the quantization effect. Quantum tunneling, also known as resonant tunneling, occurs when the applied voltage across the diode is aligned to one of the discrete energy levels in the well resulting in sharp current peak [28]. Schematic band diagrams at four different voltage values across the diode are illustrated in Fig. 16. Also shown in the figure is the - characteristic of a typical RTD. It consists of a positive differential resistance (PDR) region, a negative differential resistance region, a valley region, and a second PDR region.

RTD operates in PDR Region I. The gate enters the evaluate phase when CK switches high. The RTD stays in the PDR Re- gion I until the input voltage to the pull-down network is high enough such that the discharge current exceeds , the peak cur- rent of the RTD. After this point, the gate starts to accelerate in switching because the combined effect of increasing in dis- charge current and the decrease in the pull-up current through the RTD. After the dynamic node S drops to a certain low voltage value, the PFET in the keeper is switched off allowing the dy- namic node to fully reach the ground voltage. In all, it can be observed that dynamic logic circuits designed using the proposed method maintain the following benefits that conventional domino logic gates possess:

1) area overhead is very small in comparison with other noise tolerant techniques;

2) there is no dc power consumption;

3) signals have rail-to-rail voltage swing; and

4) clocking scheme is simple and no delay element is required. It is noted that cointegrating resonant tun- neling devices with conventional CMOS technologies is cur- rently still a challenge.

NOISE MARGIN AND DELAY ANALYSIS

In this section, we analytically study the noise margin as well as the discharge time of domino logic gates with the proposed NDR keepers. For simplicity of analysis, we assume the - characteristic of the NDR keeper can be modeled using a piece- wise linear waveform as shown in Fig. 17(a), where is the peak current, is the peak voltage, and is the voltage when the current first becomes negligible. The input signal is assumed to have a saturated ramp waveform with a rise time of . To facilitate manual analysis, we have further assumed this ramp input can be approximated by a step waveform, as shown in Fig. 17(b), where the sizes of the shadowed areas are matched.

Noise Margin Analysis

Let us consider a noise input that partially turns on the n-net- work of the dynamic logic gate. As long as the discharge current caused by the input noise does not exceed the peak

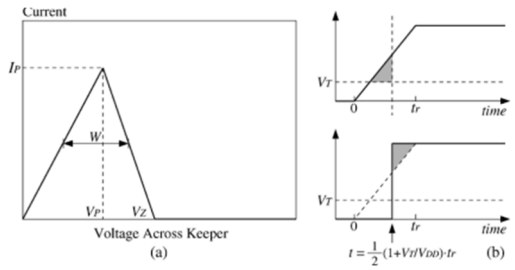


Fig17. Assumption for simple analysis. (a) Piecewise linear NDR keeper I-V characteristic. (b) Input voltage waveform (top: saturated ramp waveform; bottom: equivalent step waveform).

keeper, the keeper operates in PDR region. The voltage drop at the dynamic node S is less than or equals to and the output of the gate driver remains low. However, when the input noise voltage is large so that the discharge current of the n-network is greater than , the keeper operating point moves into the NDR region. The current supplied by the keeper reduces steeply and the voltage at the dynamic node S quickly drops resulting in a low-to-high switching of the gate driver. Overall, the maximum input noise level that the dynamic gate can withstand is the voltage that causes the voltage level at the dynamic node S to drop to .

We assume the current of the n-network of a dynamic logic gate G can be formulated using the following simple expression: the latest switching input reaches half of the supply voltage to when the dynamic node S falls to half of the supply voltage. First, referring to Fig. 17(b), the time between when the original saturated ramp input reaches half of the supply voltage and when the step waveform rises is calculated as

t_0

Next, the operation of dynamic logic gates with the proposed keeper can be divided into three stages depending on the operating regions of the keeper. In the first stage, the keeper device operates in PDR region, and the governing equation for thedy- namic node S is

wh er e is the discharge current of the pulldown n-network when it switches fully on. The above equation shows that the gate noise margin is proportional to , the peak keeper current. When the maximum input noise level is specified in a design, the keeper peak current that is necessary to meet the noise specification can be derived from (4)

I_P (5)

$I V$

The above simple equation can be used to quickly estimate the size of the keeper device.

Delay Analysis

In this section, we study the discharge time of dynamic gates with NDR keeper, where the gate delay is measured from when nodal capacitance at S. The above first-order

differential equa- tion can be solved to obtain the time for to drop from to

$t_1 = C\frac{V_P}{I_P}\ln\left(\frac{I_0}{I_0 - I_P}\right)$ (8)

In the second stage, the keeper operates in the NDR region. The time to discharge the dynamic node S from

$t_2 = C\frac{V_Z - V_P}{I_P}\ln\left(\frac{I_0}{I_0 - I_P}\right)$ (9)

In the third stage, the keeper current is negligible. The time to discharge the dynamic node S from to is simply

calculated as

$t_3 = \frac{C\left(\frac{V_{DD}}{2} - V_Z\right)}{I_0}$. (10)

The total discharge time is therefore the sum of the above four terms, which can be simplified to

$$t_d = \frac{V_T}{2V_{DD}} t_r + C\frac{V_Z}{I_P} \ln\left(\frac{I_0}{I_0 - I_P}\right) + \frac{C\left(\frac{V_{DD}}{2} - V_Z\right)}{I_0}. \quad (11)$$

It can be shown that given , the discharge time calculated using the above equation rises monotonically when the cut-off voltage increases. This is in accordance with the intuition that one needs to reduce the area beneath the - characteris- tics of the keeper device in order to minimize the performance penalty. Equation (11) can be written in the following form:

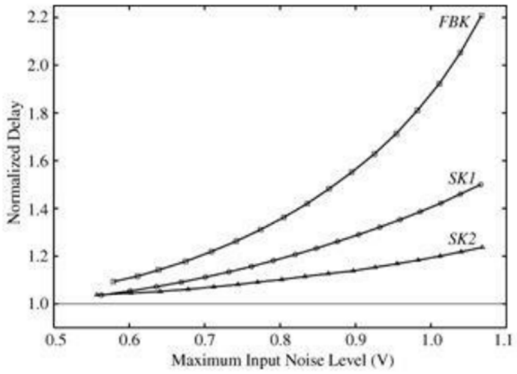


Fig20. Comparison of waveforms of domino logic gates with different keepers under noisy input

Where is the width of the current peak in the -plot as shown in Fig. 17 and is a sensitivity metric of gate delay with respect to. For realistic circuit parameters, is positive definite meaning that designers should strike for smaller values in order to minimize the performance overhead of using the keeper. The ideal case is when the width of the current peak approaches zero. Now despite the presence of the keeper with a peak current of , the total discharge time is reduced to , which is the same as the discharge time without any keeper. Intuitively, this is the case when the area bounded by the - characteristics of the keeper is negligible, meaning the effective delay keeper strength approaches zero.

EXPERIMENTAL RESULTS

In this section, we describe the simulation results for a number of wide domino logic gates with the conventional keeper and with the proposed smart keepers. The circuits are designed using a 0.18- m process technology and the simula- tion is carried out using HSPICE at 1.6 V supply voltage and at a temperature of 55 C.

We first study how gate delay increases when the gate noise robustness level is raised by adjusting keeper size. An 8-input domino OR gate is used as the test vehicle in this study. The load capacitance of the gate is 50 fF and the clock frequency used in the simulation is 500 MHz. The normalized gate delay versus maximum input noise voltage level plot obtained through SPICE simulations is shown in Fig. 18, where SK1 refers to the MOSFETbased smart keeper and SK2 refers to the RTD+FET

TableiI. Performance Comparison for Or8 At Same Noise Robustness Level

Noise Level (V)	Feedback Keeper (FBK)		Smart Keeper 1 (SK1)		Smart Keeper 2 (SK2)	
	Delay (ps)	Power (μW)	Delay (ps)	Power (μW)	Delay (ps)	Power (μW)
0.6	121.8 (10.7%)	149.5	115.9 (5.4%)	141.0	114.9 (4.5%)	151.5
0.7	132.9 (20.8%)	158.7	122.3 (11.2%)	144.5	117.4 (6.7%)	158.1
0.8	149.0 (35.5%)	172.7	130.8 (18.9%)	149.3	121.1 (10.1%)	164.1
0.9	171.9 (56.3%)	193.3	141.5 (28.6%)	155.5	125.3 (13.9%)	176.4
1.0	207.0 (88.2%)	225.1	154.6 (40.5%)	163.4	131.2 (19.3%)	190.5

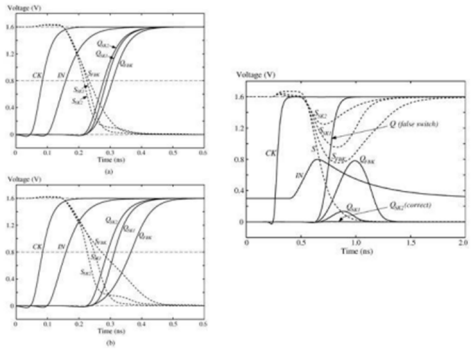


Fig19. Comparison of waveforms of domino logic gates with different keepers. (a) Noise-tolerance level at 0.8 V. (b) Noise-tolerance level at 1.0 V.

The keepers such that the resulting dynamic logic gates have same noise tolerance level. The transient waveforms when the inputs are normal signals are compared in Fig. 19. The noise- tolerance levels of the domino gates in Fig. 19(a) and (b) are 0.8 V and 1.0 V, respectively. It is observed that the dynamic nodes of the three circuits discharge approximately at the same rate initially. The difference is that both and have an accelerated discharge process after the voltage drops below about 1.2 V due to the reduced keeper current. Therefore, in addition to the reduction in IN to S delay, the S to Q delay is also decreased because of the faster input slope seen by the output driver. Overall, at same noise immunity level, dynamic logic gates using the proposed keepers switch considerably faster than their counterparts using conventional feedback keeper.

In the second experiment, we have sized the keepers such that the delay penalty over domino gate without any keeper is no more than 10%. The transient waveforms of the domino gates when the inputs are noisy signals are compared in Fig. 20. We have used an input noise waveform that is composed of both a dc component and an ac component to simulate real noise waveforms, as shown in the figure. The domino gate without keeper fails to operate correctly when this input noise is applied. Using the conventional feedback keeper, the gate output eventually reaches the correct value. However, the output of the domino gate has a large noise pulse, which, when combined with other injected noises like interconnect crosstalk noise at the output node, will lead to potential noise violation at the next gate. The output noise glitch is greatly reduced using Smart Keeper 1. And the output of the domino gate employing Smart Keeper 2 is correct and noise-free.

Logic gates are known to behave as low-pass filters. Gate noise immunity is considerably better against narrow noise pulses. Dynamic noise rejection curve is determined by the locus of the combination of input noise amplitude and duration that cause a gate to switch. An input noise will cause circuit failure if and only if the amplitude and duration combination of the noise lies above the dynamic noise rejection curve. In Fig. 21, the dynamic noise rejection curves of domino gates with different keepers are compared. The rejection curves of the proposed keepers are always higher than that of the feedback keeper meaning that they have higher noise immunity.

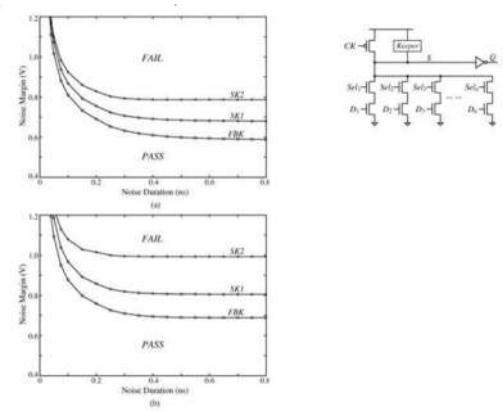


Fig21. Dynamic noise rejection curves. (a) When delay overhead is 10%. (a)When delay overhead is 20%.

It is also observed that the difference in dynamic noise immunity among the keepers are reduced when the input noise duration is extremely small. This is essential for high performance operation of dynamic logic gates employing the proposed keepers. This is because there is no real difference between an input noise with very high amplitude ( )

and a narrow duration and the initial portion (from 0 to) of a normal input. Therefore, the delay overhead will be at least if the combination (,) is below the dynamic noise rejection curve.

Experimental results also support that the noise tolerance of dynamic logic gates can be improved beyond the level of static CMOS logic gates while their advantage in performance is still retained. This is mainly due to the fact that dynamic logic cir- cuits have a single polarity. Input noise signals are of either the low-high-low type of the highlow-high type. For static CMOS gates, when noise tolerance against one type of noise is improved, the noise tolerance against the other type of noise is al- ways adversely affected. For dynamic logic gates, on the other hand, one can aggressively improve gate noise tolerance against the interested type of noise without having to worry about the other type.

CONCLUSIONS Effective noise-tolerant design techniques are vital to the success of VLSI circuits as noises become an ever-increasing problem with the relentless scaling of process technology. A desirable noise-tolerant technique should be able to improve circuit robustness against all noise types, be suitable for all logic functions, and have very low overhead in silicon area, circuit speed, and power consumption. In this paper, such a noise-tolerant design technique is proposed.

TableIII. Performance Comparison For Muxes At Same Noise Robustness Level

Noise Level (V)	MUX (bit)	Feedback Keeper (FBK)		Smart Keeper 1 (SK1)		Smart Keeper 2 (SK2)	
		Delay (ps)	Pwr (μW)	Delay (ps)	Pwr (μW)	Delay (ps)	Pwr (μW)
0.6	8	136.7 (11.7%)	145.8	128.3 (4.8%)	137.2	127.1 (3.8%)	147.4
	16	159.5 (10.1%)	160.9	151.5 (4.6%)	151.2	150.0 (3.5%)	161.5
	32	203.1 (9.4%)	192.7	194.1 (4.6%)	181.3	191.6 (3.2%)	191.4
0.7	8	150.5 (23.0%)	156.0	136.2 (11.3%)	140.9	129.9 (6.1%)	153.8
	16	176.2 (21.6%)	172.5	159.3 (9.9%)	155.0	153.2 (5.7%)	168.0
	32	223.9 (20.6%)	206.9	204.5 (10.2%)	186.2	196.0 (5.6%)	197.9
0.8	8	175.6 (43.5%)	173.4	147.6 (20.6%)	146.4	134.3 (9.7%)	161.9
	16	204.4 (41.1%)	192.3	170.6 (17.7%)	160.5	158.3 (9.2%)	176.4
	32	258.7 (39.4%)	231.6	218.9 (17.9%)	193.3	202.9 (9.3%)	206.5
0.9	8	220.2 (79.9%)	204.2	163.4 (33.5%)	154.1	139.6 (14.1%)	177.4
	16	254.6 (75.7%)	227.6	185.8 (28.2%)	167.9	164.3 (13.4%)	182.2
	32	320.9 (72.9%)	275.9	238.5 (28.5%)	203.1	210.6 (13.5%)	222.8
1.0	8	333.7 (172.6%)	282.6	185.4 (51.5%)	164.8	146.8 (19.9%)	196.6
	16	383.1 (164.4%)	318.4	205.7 (42.0%)	177.8	172.4 (19.0%)	211.5
	32	479.6 (158.4%)	392.2	264.6 (42.6%)	216.3	221.4 (19.3%)	242.7

The main contributions of this paper are as follows. First, we have identified the difference between keeper strength for noise immunity and keeper strength for speed, which opensthe possibility for circuit noise immunity improvement without a proportional increase in delay. Second, we have proposed to use a class of circuits having the folded-back - characteristic (the NDR property) to explore the difference in keeper strength for speed and for noise immunity. And third, we have proposed two circuit realizations of the NDR keeper and have demonstrated the potential benefit of the proposed technique.

More specifically, we have shown that the proposed tech- nique improves dynamic circuit noise immunity with little cost in area, speed, and power consumption. Simulation results on large fan-in domino gates have shown that, at a supply voltage of 1.6 V, the dc input noise voltage level can be raised to 0.8 V for about 10% delay overhead and to 1.0 V for about 20% delay overhead. Furthermore, in contrast to most existing noise tolerance enhancing remedies, the proposed technique does not modify/change the pull-down transistor network. Therefore it is easier to be adopted in circuit design practice. We have also shown that it will be more rewarding to use the proposed tech- nique as the process technology continues to scale down and the noise problem becomes more prominence.

The proposed technique is not limited to domino logic gates. It can also be applied to other combinational dynamic logic cir- cuits as well as sequential circuits like latches and flipflops that have internal precharged nodes. This constitutes one direction of future researches. In the other direction, we will also search for other suitable circuit implementations that aggressively ex- plore the benefit of the noisetolerant design principle described in this paper.

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